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Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-22. Canceled

23.   (New) A method of accessing a nonvolatile semiconductor memory in a memory card comprising:

receiving a first logical block address corresponding to a first physical block address in a first memory zone, the first memory zone including a first plurality of physical memory blocks;

generating a first address translation table, in volatile memory, for the first memory zone;

receiving a second logical block address corresponding to a second physical block address that is within a second memory zone including a second plurality of physical memory blocks;

checking whether the second logical address is within the first memory zone; and

if the second logical block address is not within the first memory zone, generating a second address translation table, in the volatile memory, for the second memory zone.

24.   (New) A method according to claim 23, wherein the first and second address translation tables are generated by referring to information stored in the nonvolatile semiconductor memory.

25.   (New) A method according to claim 24, further comprising a step of calculating an offset logical block address within the second memory zone from the second logical block address.

26.   (New) A method according to claim 25, wherein the nonvolatile semiconductor memory is a NAND flash memory.

27.   (New) A method according to claim 25, wherein the nonvolatile semiconductor memory is a NAND flash memory with four-level memory cells.

28.   (New) A method according to claim 26, wherein the first memory zone and the second memory zone reside within a single semiconductor chip.

29.   (New) A method according to claim 27, wherein the first memory zone and the second memory zone reside within a single semiconductor chip.

30.   (New) A method of accessing a nonvolatile semiconductor memory in a memory card comprising:

receiving a first logical block address corresponding to a first physical block address in a first memory zone, the first memory zone including a first plurality of physical memory blocks, the first memory zone reserved for storing file management information;

generating a first address translation table, in volatile memory, for the first memory zone;

receiving a second logical block address corresponding to a second physical block

address that is within a second memory zone including a second plurality of physical memory

blocks, the second memory zone reserved for storing user data;

checking whether the second logical block address is within the first memory zone; and

if the second logical block address is not within the first memory zone, generating a

second address translation table, in the volatile memory, for the second memory zone without

superseding the first address translation table in the volatile memory.

31.   (New) A method according to claim 30, wherein the file management

information includes a file allocation table or directory information.

32.   (New) A method according to claim 31, wherein the first and second address

translation tables are generated by referring to information stored in the nonvolatile

semiconductor memory.

33.   (New) A method according to claim 32, further comprising a step of calculating

an offset logical block address within the second memory zone from the second logical block

address.

34.   (New) A method of claim 33, wherein the nonvolatile semiconductor memory is

a NAND flash memory.

35.   (New) A method according to claim 33, wherein the nonvolatile semiconductor memory is a NAND flash memory with four-level memory cells.

36.   (New) A method according to claim 34, wherein the first memory zone and the second memory zone reside within a single semiconductor chip.

37.   (New) A method according to claim 35, wherein the first memory zone and the second memory zone reside within a single semiconductor chip.